## REMARKS

### Drawings

The Examiner has rejected to Figure 1 because it is the Examiner's position that it should be designated by a legend, such as "Prior Art" because only that which is old is illustrated. Applicant submits herewith a proposed drawing correction, in red, to Figure 1 designating the legend "Prior Art".

The Examiner has objected to the drawings as failing to comply with 37 CFR 1.84(p)(4) because a reference character "302" has been used to designate both n-well and p-well. Applicant has amended the specification on page 13, line 27 to indicate that the substrate includes an n-well 302.

The Examiner has objected to the drawings as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: element 324. Included herewith is a proposed drawing correction, in red, to Figure 8 setting forth element 324.

### Specification

The Examiner has objected to the disclosure because of the following imformalities: on page 9, line 16 the word "then" should be "than". Applicant provides herewith an amendment to the specification to clarify the typographical error.

### Claim Objections

The Examiner has objected to claim 4 because of the following informalities: the word "then" should be "than". Additionally, the Examiner has objected to claim 10 because of the following informalities: the "method" should be "product" based on dependency to claim 1. Applicant has amended claims 4 and 10 as well as other claims to more particularly point out and distinctly claim the subject matter which Applicant regards as the invention. The amendment are for clarity purposes and do not further limit the present invention.

**Claim Rejections - 35 U.S.C. § 102/103**

The Examiner has rejected claims 1, 8, 9, and 12 under 35 U.S.C. 102(b) as being anticipated by Krivokapic (US Patent 5,824,587). The Examiner has rejected claim 13 under 35 U.S.C. 102(e) as being anticipated by Takeuchi (US Patent 5,970,351). The Examiner has rejected claim 15 under 35 U.S.C. 102(e) as being anticipated by Choi (US Patent 6,057,582). The Examiner has rejected claim 2 under 35 U.S.C. 103(a) as being unpatentable over Krivokapic (US Patent 5,824,587). The Examiner has rejected claim 3 under 35 U.S.C. 103(a) as being unpatentable over Krivokapic '587. The Examiner has rejected claim 4 under 35 U.S.C. 103(a) as being unpatentable over Krivokapic in view of Takeuchi '351 as applied to claim 2 above. The Examiner has rejected claims 5 and 6 under 35 U.S.C. 103(a) as being unpatentable over Krivokapic '587 in view of Choi et al. (US Patent 5,793,088). The Examiner has rejected claims 7, 10, and 11 under 35 U.S.C. 103(a) as being unpatentable over Krivokapic '587. The Examiner has rejected claim 14 under 35 U.S.C. 103(a) as being unpatentable over Takeuchi '351 in view of Choi "582.

It is Applicant's understanding that the cited references fail to teach or render obvious Applicant's invention as claimed in claims 1-14. In claims 1-14, Applicant claims a novel MOS transistor structure with improved performance and scalability.

According to the present invention, the structure includes inwardly concaved source/drain regions formed with deposited silicon or silicon alloys. The inwardly concaved source/drain regions created a channel region with is larger at the silicon/gate oxide interface and narrower deeper into the substrate. With this geometry, a larger channel length ($L_{met}$) is achieved during the "off state" while a smaller $L_{met}$ is achieved during the "on state". In an embodiment of the present invention, the device includes a gate dielectric which is thicker at the extension or tip overlap region which improves the robustness of the gate oxide gate leakage. In an embodiment of the present invention, the device includes raised source/drain regions having a (311) facet which helps reduce the fringing capacitance of the device. The novel feature of the present invention, such as inwardly concaved source/drain regions, thicker gate oxide at the gate edge and raised source/drain regions with engineered facet can be used in combination with one another to provide an MOS device with improved short channel effects, reduced gate edge leakage, and reduced over lap capacitance.

The inwardly concaved source/drain regions are formed by isotropically etching recesses 312 into a substrate 302 in order to form an inflection point 315 as shown in Figure 6. The recesses are then filled with a deposited silicon or silicon alloy layer 318, such as silicon germanium, as shown in Figure 7.

It is Applicant's understanding that neither Krivokapic, Takeuchi or Choi teach a source/drain region formed from a deposited silicon or silicon alloy and constructed to define a channel region in the substrate directly beneath the gate electrode which is larger than the channel region deeper into the substrate, as claimed by Applicant .

It is Applicant's understanding that Krivokapic describes source/drain regions 217 and 218 formed into a convex 224 surface of silicon substrate 201. The source/drain regions 217 and 218 are formed by diffusing dopants from silicon layer 234 into substrate 201. Thus, source/drain regions 217 and 218 are formed of doped

regions of semiconductor substrate 201 and not of deposited silicon or silicon alloy as claimed by Applicant. Additionally, Takeuchi also teaches source/drain regions formed by diffusing dopants into the substrate. Choi also teaches source/drain regions (25/27) formed by doping regions of substrate 21. As such, neither Krivokapic, Takeuchi nor Choi teach a source/drain regions formed from deposited silicon and creating a channel region directly beneath the gate electrode which is larger than the channel region deeper into the substrate.

As such, the cited reference either alone or in combination fail to teach or render obvious Applicant's invention as claimed in claims 1-14. Applicant therefore respectfully requests the removal of the 35 U.S.C. 102 and 103 rejections of claims 1-14 and seeks an early allowance of these claims.

## VERSION WITH MARKINGS TO SHOW CHANGES MADE

## IN THE SPECIFICATION

Please replace paragraph starting on page 9 line 16 with the following paragraph:

The n-type region 206 located between the source/drain extensions 242 defines the channel region 250 of device 200. As shown in Figure 2, the source/drain regions are formed with a recess etch which creates a source/drain extension geometry which concaves inward creating an inflection point 260. The inflection point 260 is the location where the source/drain regions extend the greatest lateral distance beneath of gate electrode 202. In this way, when the recesses are back filled with highly conductive silicon or silicon alloy the distance between the source/drain extension regions is larger directly beneath the gate dielectric than is the distance deeper into the n-type region. That is, in accordance with an embodiment of the present invention source/drain regions are formed in a manner which creates a channel region 252 directly beneath the gate dielectric with a larger physical or metallurgical channel length ($L_{met}$) **[then]** **than** the channel region 254 deeper into the substrate between the inflection points 260. Such a unique geometry provides improved performance in both the "on" and "off" states of the device. When the device is "off", the channel region remains n-type (no inversion). In the off condition any leakage ($I_{off}$) is due to holes traveling from the source/drain extension region to the other source/drain extension region directly beneath the gate oxide in region 252. In the off condition, holes experience a large channel length which greatly reduces the leakage current (i.e., reduces $I_{off}$). On the other hand, when device 200 is in the "ON" condition, n-type region 206 forms a channel by inverting the n-type silicon into p-type silicon. The inversion region forms a channel deeper into the substrate than the depth at which the inflection point 260 occurs. In this way, when the

device is in the "on" condition and the inverted channel formed, a smaller $L_{met}$ is realized. A smaller $L_{met}$ during the "ON" state directly translates to a smaller channel resistance which results in a higher $I_{on}$.

Please replace paragraph starting on page 13 last line with the following paragraph:

According to the present invention a thin spacer layer 308 is formed over substrate 300 including **[p-well]** **n-well** 302 and the top and sides of gate electrode 306 as shown in Figure 4. Spacer layer 308 will subsequently be used to form sidewall spacers for the MOS device. Spacer layer 310 is formed to a thickness between 50-300Å. It is to be appreciated that spacer layer 308 must be formed thick enough to electrically isolate a subsequently deposited silicon or silicon alloy film from gate electrode 306.

Please replace paragraphs starting on page 19 line 16with the following paragraph:

Next, as shown in Figure 8, a thin, approximately 50-100Å chemical vapor deposited (CVD) oxide layer 322 is blanket deposited over substrate 300 including silicon or silicon alloy film 318, sidewall spacers 310 and isolation regions 304. Oxide layer 322 can be formed by any well known CVD process. In a preferred embodiment however the deposition temperature is kept below 750°C in order to not activate or disturb the dopants in the silicon or silicon alloy. An oxide deposition temperature of approximately 650°C is preferred. Next, a substantially thicker, 500 to 1800Å with 800Å, CVD silicon nitride layer 324 is blanket deposited onto oxide layer **[320]** **322**. Silicon nitride layer 324 is preferably formed by a standard CVD "hot wall" process at a temperature below 750°C and a temperature of 750°C being ideal. By keeping the silicon nitride deposition temperature relatively low the thermal budget is kept down and the deposition rate and uniformity made more controllable. Oxide layer **[320]**

322buffers the large stress inherent silicon nitride layer [322] 324 and provides an etch step for silicon nitride layer [322] 324 during a subsequent spacer etch.

Next, silicon nitride layer [322] 324, and oxide layer [320] 322, are anisotropically etched to form a pair of composite spacers 326 adjacent to the first pair of silicon nitride spacers 310 as shown in Figure 9. Any well known silicon nitride and oxide etchant process may be used to anisotropically etch silicon nitride layer [322] 324 and buffer oxide layer [320] 322. Additionally, it is to be appreciated that although composite spacers are utilized a single nitride or oxide layer can be used to form spacers 326 if desired. Spacers 326 are used to separate a silicide on the source/drain regions from a silicide on the gate region and/or to offset a high energy high dose implant from the active channel region. In an embodiment of the present invention spacers 326 have a thickness between 500-2000Å.

## IN THE CLAIMS

1. (Amended) An MOS device comprising:

a gate dielectric formed on first conductivity region in a substrate;

a gate electrode formed on said gate dielectric;

a pair of sidewall spacers formed along laterally opposite sidewalls [in] of said gate electrode; and

a pair of deposited silicon or silicon alloy source/drain regions of a second conductivity type formed in said substrate and on opposite sides of said gate electrode, wherein said silicon or silicon alloy source/drain regions extend beneath the gate electrode and [defining] define a channel region beneath said gate electrode in said first conductivity type region, and wherein said channel region directly beneath said gate electrode is larger than said channel region deeper into said first conductivity type region.

6. (Amended) The MOS device of claim 5 wherein the concentration of said deposited silicon or silicon alloy regions having a [first] conductivity type is greater than the concentration of said first conductivity type region.

10. (Amended) The [method] MOS device of claim 1 wherein the concentration of said deposited silicon or silicon alloy source/drain regions of a second conductivity type have a concentration between $1x10^{18}/cm^3 - 3x10^{21}/cm^3$.

13. (Amended) An MOS device comprising:

a gate dielectric formed on a first conductivity type region in a substrate;

a gate electrode formed on said gate dielectric;

a pair of sidewall spacers formed along laterally opposite sidewalls of said gate electrode; and

a pair of deposited silicon or silicon alloy source/drain regions having a second conductivity type formed in said substrate and along opposite sides of0 said gate electrode wherein said deposited silicon or silicon alloy extends above the height of said gate dielectric layer wherein the top surface of said deposited silicon or silicon alloy is spaced further from said gate electrode than said silicon or silicon alloy adjacent to said gate dielectric.